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1 **Managing static leakage energy in microprocessor functional units**
Dropsho, S.; Kursun, V.; Albonesi, D.H.; Dwarkadas, S.; Friedman, E.G.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Pages:321 - 332

[Abstract] [PDF Full-Text (362 KB)] **IEEE CNF**

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2 **Overview of complementary GaAs technology for high-speed VLSI circuits**
Brown, R.B.; Bernhardt, B.; LaMacchia, M.; Abrokwah, J.; Parakh, P.N.; Basso, T.D.; Gold, S.M.; Stetson, S.; Gauthier, C.R.; Foster, D.; Crawforth, B.; McQuire, T.; Sakallah, K.; Lomax, R.J.; Mudge, T.N.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 6 , Issue: 1 , March 1998
Pages:47 - 51

[Abstract] [PDF Full-Text (108 KB)] **IEEE JNL**

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3 **A high-speed asynchronous decompression circuit for embedded processors**
Benes, M.; Wolfe, A.; Nowick, S.M.;
Advanced Research in VLSI, 1997. Proceedings., Seventeenth Conference on , 15-16 Sept. 1997
Pages:219 - 236

[Abstract] [PDF Full-Text (1064 KB)] **IEEE CNF**

4 **Flow-through latch and edge-triggered flip-flop hybrid elements**
Partovi, H.; Burd, R.; Salim, U.; Weber, F.; DiGregorio, L.; Draper, D.;
Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996 IEEE International , 8-10 Feb. 1996
Pages:138 - 139

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

5 **A 150-mW subscriber-line-board controller**
Van Simaeys, F.C.; Guebels, P.; Rahier, M.C.; Van De Weghe, H.; Huyskens, E.G.;
Solid-State Circuits, IEEE Journal of , Volume: 21 , Issue: 2 , Apr 1986
Pages:259 - 266

[Abstract] [PDF Full-Text (1016 KB)] **IEEE JNL**

6 **Low-power and high-speed ROM modules for ASIC applications**
Ching-Rong Chang; Jinn-Shyan Wang; Cheng-Hui Yang;
Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 10 , Oct. 2001
Pages:1516 - 1523

[Abstract] [PDF Full-Text (304 KB)] **IEEE JNL**

7 **Capacitor coupling threshold logic**
Jia, C.; Milor, L.; Huang, H.-Y.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 1 , 4-7 Aug. 2002
Pages:I - 483-6 vol.1

[Abstract] [PDF Full-Text (307 KB)] **IEEE CNF**

8 **A novel latch design technique for high speed GaAs circuits**
Nooshabadi, S.; Montiel-Nelson, J.A.; Eshraghian, K.;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on , Volume: 1 , 5-8 Sept. 1999
Pages:331 - 334 vol.1

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Hazard-free implementation of speed-independent circuits

Kondratyev, A. Kishinevsky, M. Yakovlev, A.
Aizu Univ., Japan;

This paper appears in: **Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on**

Publication Date: Sept. 1998
On page(s): 749 - 771
Volume: 17 , Issue: 9
ISSN: 0278-0070
Reference Cited: 43
CODEN: ITCSDI
Inspec Accession Number: 6041724

Abstract:
This paper develops a theoretical framework for the hazard-free gate-level implementation of speed-independent circuits specified by event-based models, such as signal transition graphs (for processes with AND causality and input choice) or their extension, called change diagrams (which allow OR-causality). It presents sufficient conditions, called the generalized monotonous cover requirements, for a hazard-free circuit to be built within a standard implementation structure. This structure consists of two-level simple-gate combinational logic and a row of latches, either a C-element or an RS-latch. A set of semantic-preserving transformations is defined that can be applied to an original behavioral description of the circuit so as to produce its specification in the form that satisfies the monotonous cover requirement. The transformations are applied at the event-based representation level (to avoid state explosion) and proved to be effective. The main result of the paper is therefore twofold: 1) the proof that any speed-independent behavior can be implemented at the gate level without hazards and 2) an efficient method for constructing such an implementation. Experimental results show that the proposed method compares very favorably, in area and performance, to the previously known techniques

Index Terms:
asynchronous circuits combinational circuits hazards and race conditions logic CAD signal flow graphs AND causality C-element OR-causality RS-latch asynchronous circuits behavioral description change diagrams event-based models gate-level implementation generalized monotonous cover requirements hazard-free implementation latches logic synthesis semantic-

preserving transformations signal transition graphs speed-independent circuits two-level simple-gate combinational logic

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Benes, R.; Nowick, S.M.; Wolfe, A.;
Advanced Research in Asynchronous Circuits and Systems, 1998. Proceedings. 1998 Fourth International Symposium on , 30 March-2 April 1998
Pages:43 - 56

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[Abstract] [PDF Full-Text (521 KB)] **IEEE CNF**

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1 **Relative timing [asynchronous design]**
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Pages:1466 - 1477

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9 **Power management in the Amulet microprocessors**
Furber, S.B.; Efthymiou, A.; Garside, J.D.; Lloyd, D.W.; Lewis, M.J.G.; Temple, S.;
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10 **Coming challenges in microarchitecture and architecture**
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Pages:325 - 340

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11 **Subject Index**

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Pages:1864 - 1902

[Abstract] [PDF Full-Text (282 KB)] IEEE JNL

12 **Subject Index**

Proceedings of the IEEE , Volume: 88 , Issue: 12 , Dec. 2000
Pages:INDEX_13 - INDEX_52

[Abstract] [PDF Full-Text (316 KB)] IEEE JNL

13 **A self-timed real-time sorting network**
Yun, K.Y.; James, K.W.; Fairlie-Cuninghame, R.H.; Chakraborty, S.; Cruz, R.L.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 8 , Issue: 3 , June 2000
Pages:356 - 363

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1 **A fast asynchronous Huffman decoder for compressed-code embedded processors**
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16 **A result forwarding mechanism for asynchronous pipelined systems**
Gilbert, D.A.; Garside, J.D.;
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17 **ASYNMPU: a fully asynchronous CISC microprocessor**
Tse, J.M.C.; Lun, D.P.K.;
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Pages:1816 - 1819 vol.3

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18 **Synchronous implementation of a counterflow pipeline processor**
Janik, K.J.; Shih-Lien Lu;
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Pages:69 - 72 vol.4

[Abstract] [PDF Full-Text (228 KB)] **IEEE CNF**

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19 **A CMOS floating point multiplier**
Uya, M.; Kaneko, K.; Yasui, J.;
Solid-State Circuits Conference. Digest of Technical Papers. 1984 IEEE International , Volume: XXVII , Feb 1984
Pages:90 - 91

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

20 **The design of an asynchronous TinyRISC™ TR4101 microprocessor core**
Christensen, K.T.; Jensen, P.; Korger, P.; Sparso, J.;
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21 **Writing sequential programs for parallel processors: implementation experience**
Subramonian, R.;
Computing and Information, 1992. Proceedings. ICCI '92., Fourth International Conference on , 28-30 May 1992
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1 **Shaping codes constructed from cost-constrained graphs**
McLaughlin, S.W.; Khayrallah, A.S.;
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[Abstract] [PDF Full-Text (292 KB)] **IEEE JNL**

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[Abstract] [PDF Full-Text (252 KB)] **IEEE JNL**

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1 **Lazy transition systems and asynchronous circuit synthesis with relative timing assumptions**
Cortadella, J.; Kishinevsky, M.; Burns, S.M.; Kondratyev, A.; Lavagno, L.; Stevens, K.S.; Taubin, A.; Yakovlev, A.;
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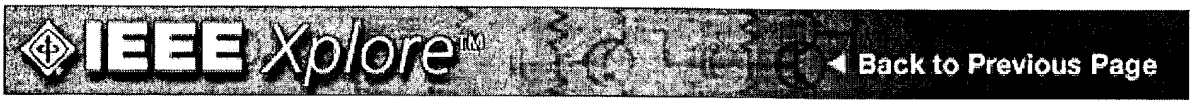
[Abstract] [PDF Full-Text (511 KB)] **IEEE JNL**



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16 **Asynchronous datapath with software-controlled on-chip adaptive voltage scaling for multirate signal processing applications**
Yee William Li; Patounakis, G.; Jose, A.; Shepard, K.L.; Nowick, S.M.;
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17 **Analysis of blocking dynamic circuits**
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18 **Proceedings 2002 Design, Automation and Test in Europe Conference and Exhibition**

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9 **Boosters for driving long onchip interconnects - design issues, interconnect synthesis, and comparison with repeaters**
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16 **Asynchronous datapath with software-controlled on-chip adaptive voltage scaling for multirate signal processing applications**
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Asynchronous Circuits and Systems, 2003. Proceedings. Ninth International Symposium on , 12-15 May 2003
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[Abstract] [PDF Full-Text (2330 KB)] **IEEE CNF**

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[Abstract] [PDF Full-Text (365 KB)] **IEEE CNF**

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